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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/629,085	07/31/2000	Peter C. Damron	SUN-P4935	4971

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EXAMINER	
BRAGDON, REGINALD GLENWOOD	
ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 02/10/2004 10

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/629,085	Applicant(s) DAMRON, PETER C.	
	Examiner Reginald G. Bragdon	Art Unit 2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 14-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12 December 2003 has been entered.

Claim Objections

2. Claims 2, 4-6, 10, 17, 22, and 24-26 are objected to because of the following informalities:

As per claims 2, 4, 6, 10, 17, 22, 24, and 26line 4, --in each of the plurality of processors-- should be added after "TLB".

All dependent claims are objected to as having the same deficiencies as the claims they depend from.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3, 6-9, 11-12, 15-16, 18-21, 23, and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Traynor (6,263,403) in view of Moore et al. (5,437,017).

As per claims 1 and 8, Traynor teaches a multiprocessor system, either a snoop based system or a directory based multiprocessor system (see column 5, lines 22-29). The snoopy based system is described in column 4, lines 34-55, and the directory based system is described in column 4, line 56, to column 5, line 10. Each CPU module ("processor") contains a translation lookaside buffer (TLB). See column 1, lines 52-53. Traynor teaches the basic TLB process, where a TLB is accessed by a virtual address and generates a physical address ("accessing a virtual address..." and "locating an associated physical address"). See column 1, lines 57-64. Traynor teaches that if a translation is not in the TLB, then a page table is accessed to determine the translation, which is entered in the TLB. See column 1, line 65, to column 2, line 4.

Traynor teaches a process of purging TLB entries in processors of the multiprocessor system. A cache module requesting to change a virtual to physical address translation will generate what is generally referred to as an INVALIDATE request. See column 6, lines 29-54. In addition to the "Invalidate" instruction, the request also includes a physical address. See column 6, lines 54-55. The INVALIDATE request is broadcast to the processors in the system ("sending the TLB message..."). See column 6, lines 35-38. Each processor with a TLB determines if the physical address in the INVALIDATE request is present in it's page table and TLB. See figure 4, steps 24-26, and purges a TLB entry if the virtual address translation

corresponding to the physical address is present in the TLB ("determining..."). See step 30 of figure 4.

Furthermore, Traynor suggests that if a translation is inserted into a TLB, then the coherency protocol should be implemented. See column 7, lines 48-54. However, Traynor does not explicitly teach generating a message to entries in other TLBs of the multiprocessor system in response to removing an entry from a TLB. Moore et al. teaches that it was known to invalidate entries in other TLBs of a multiprocessor system in response to invalidating an entry in first TLB ("the second entry was removed"). See column 2, lines 25-30. It would have been obvious to one of ordinary skill in the art to have modified Traynor such that when invalidating an entry (i.e. "the second entry was removed") in a first TLB an invalidation request is sent to other TLBs in the multiprocessor system in order to maintain coherency as suggested by Moore et al. in column 2, lines 30-31.

As per claims 3, 11, 15, 18, and 23, Moore et al. teaches invalidating an entry in the other system processors.

As per claims 6-7 and 26-27, Traynor and Moore et al. teach invalidating an entry in associated TLBs. This would involve comparing the value in the INVALIDATE request with entries in the TLB and then purging when a match occurs.

As per claims 9, 12, and 20, these claims are rejected for the reasons set forth for claims 1 and 8, above, further noting that Traynor teaches that multiprocessor systems can be coupled together using a ring or crossbar network, which are both independent paths. See column 5, lines 15-17.

As per claim 16, Moore et al. teaches performing TLB invalidate operations in response to relocating ("moving") data or instructions within system memory. See column 7, lines 13-15.

As per claims 19, 21, and 28, Traynor teaches that multiprocessor systems can be coupled together using a ring or crossbar network, which are both independent paths. See column 5, lines 15-17.

5. Claims 2, 4-5, 10, 14, 17, 22, and 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Traynor in view of Moore et al. in further view of Schimmel (6,105,113).

The combination of Traynor and Moore et al. does not teach updating the TLB entry in the other processor TLBs instead of invalidating the TLB entry (updating the TLB entry involves "reading" the TLB entry when snooped, where Traynor teaches comparing the addresses to determine if an entry is in the TLB). Schimmel teaches that is was known to update entries in a TLB instead of invalidating entries. See column 4, lines 5-21. It would have been obvious to one of ordinary skill in the art to have updated the TLB entry in the other processors instead of invalidating the entry, as taught by Schimmel, because updating the entry instead of invalidating the entry would reduce TLB misses in the other TLBs.

Response to Arguments

6. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection necessitated by the amendments to the claims.

Conclusion

7. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

All "OFFICIAL" patent application related correspondence transmitted by FAX must be directed to the central FAX number at **(703) 872-9306**:

"INFORMAL" or "DRAFT" FAX communications may be sent to the Examiner at **(703) 746-5693**, only after approval by the Examiner.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Fourth Floor (receptionist).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (703) 305-3823. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Mano Padmanabhan, can be reached at (703) 306-2903.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Reginald G. Bragdon
Primary Patent Examiner
Art Unit 2188

RGB
February 5, 2004